ASIC Building Blocks for Space

MAPLD – September 2008 - Annapolis, MD

Stephan Fischer, Paul Rastetter, Richard Wiest, Uwe Hoch

EADS Astrium GmbH
81663 Munich, Germany
Tel.: +49-89-607-24256
email: Uwe.Hoch@astrium.eads.net

All the space you need

EADS astrium

Overview

- ASIC developments – Tendencies
- Astrium GmbH ASIC portfolio:
  - SpaceWire Products SMCS332SpW, SMCS116SpW
  - DICOS
  - PSIE
  - Wideband Digital Waveform Generator
  - TERESA
  - AGGA-3
  - MDPA
  - …
- Conclusion

ASIC developments – Tendencies

- ASIC complexity and gate count heavily increasing
- ASIC prices increase (price per gate decreases slowly)
- Rapid technology evolvement in commercial industry
- Trend towards deep-sub-micron ASIC technology
- More and more new technical issues arise

ASIC developments – Tendencies

- Answers:
  - Design of ASICs for a wider community (e.g. ATMEL ASSP) using standard interfaces
  - Design of Multi-Mode ASICs (reduces the number of ASIC runs)
  - Intensive use of IPs (IPs for special functions up to complex IPs like LEON2-FT or MilBus-1553)
  - Functional verification with FPGAs

ASIC developments – Tendencies

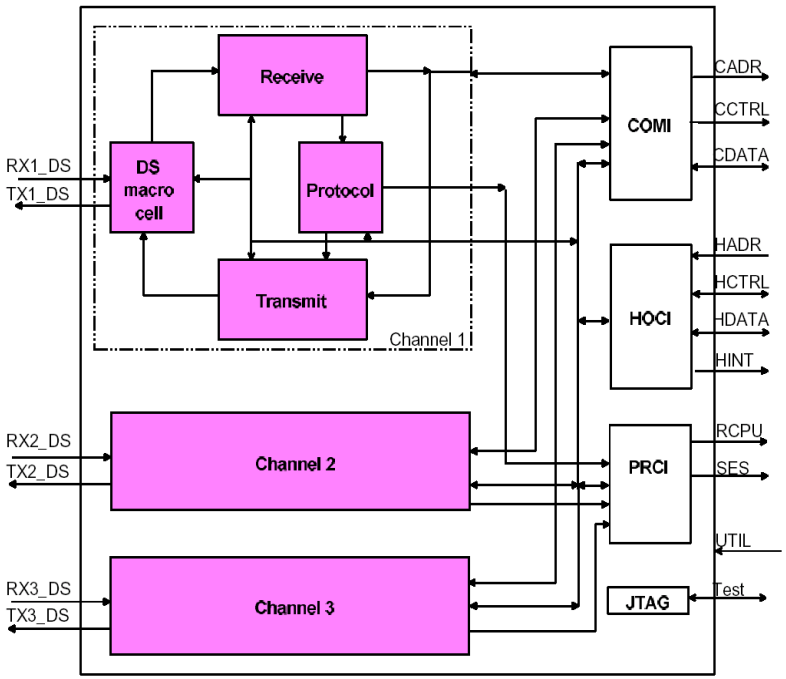
- Outlook & Need:
  - Ensure continued availability of existing space proven technology → non-DSM-ASIC sufficient for most current and future applications
  - In flight heritage of new technology & broad customer experience needed for any new technology used for space
  - Availability of standard ASICs to the complete space community as reliable baseline - coordinated by international and national agencies (and close cooperation of manufacturers and industry)

Astrium GmbH ASIC portfolio

- ASIC developments
  - SpaceWire Products SMCS332SpW, SMCS116SpW
  - DICOS (Correlation ASIC)
  - PSIE (Parallel/Serial Interface Engine)
  - Wideband Digital Waveform Generator
  - TM/TC, Reconfiguration, SGM & HKM ASIC (TeReSA)
  - AGGA3 / follow on
  - MDPA
  - …

Introduction SMCS332

- 3 bi-directional IEEE1355 link channels
  - each with DS macro cell,
  - receive, transmit section,
  - protocol processing unit



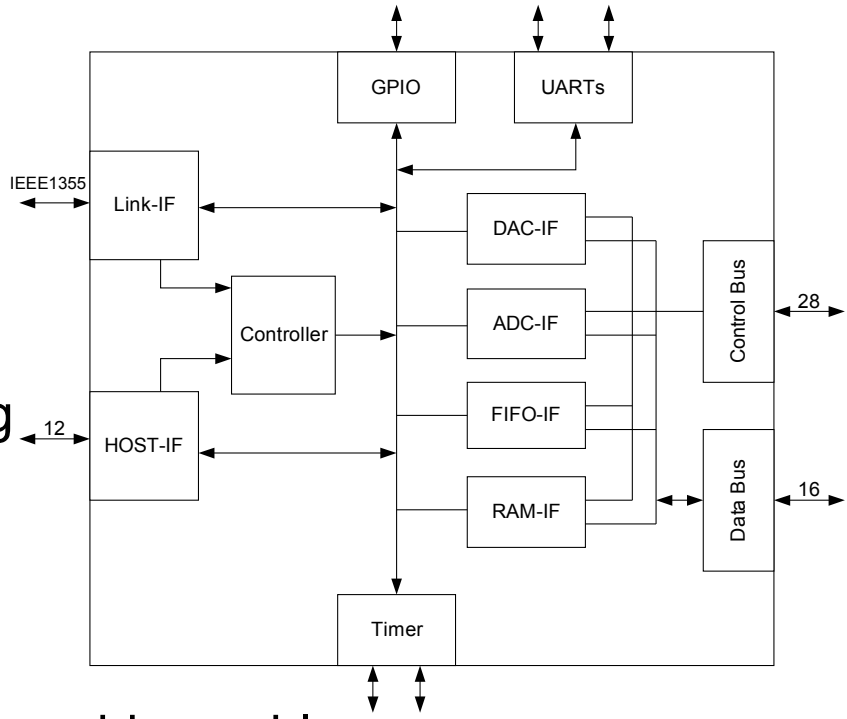
- COMI: Com Memory Interface
  - performs autonomous accesses to the communication memory

- HOCI: Host Control Interface
  - gives r/w access to configuration registers and to DS channels for the CPU

- PRCI: Protocol Command Interface collects commands from protocol units

Introduction SMCS116

- Link Interface:
  - Interface to serial IEEE-1355 link
  - controlled by Link
- Host Interface:
  - parallel Interface for programming and controlling
- ADC/DAC I/F:
  - read from ADC or write to DAC
- RAM IF:
  - 4 banks (each 64K) of memory are addressable
- FIFO I/F:
  - small internal FIFO (passive mode)
  - interface to external FIFO (active mode)
- GPIO: General Purpose Interface, up to 24 I/Os
- UART: 2 independent UARTs



SMCS332SpW, SMCS116SpW

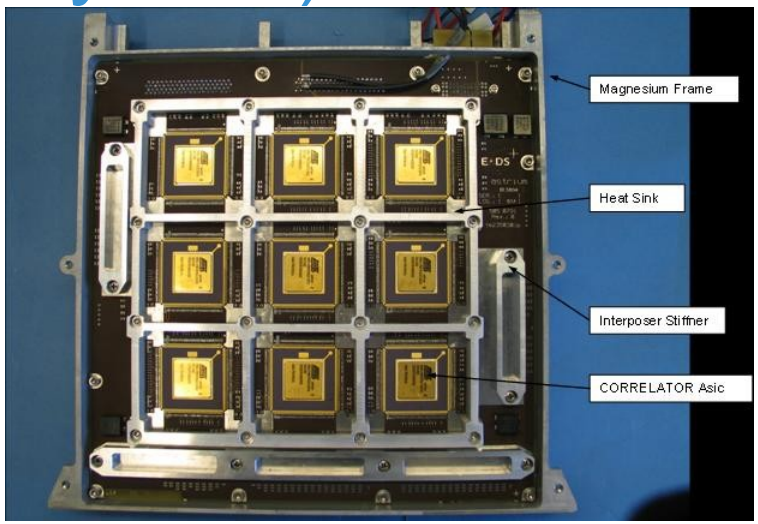
- Motivation for new SMCS SpaceWire ASICs
  - SMCS ASICs are often used communication controllers
  - SpaceWire standard is becoming increasingly important
  - ESA support
- Requirements for the new SMCS SpW
  - SpaceWire compliant (ECSS-E-50-12A, 24-Jan-2003)
  - Pin compatible to existing SMCS332 / SMCS116
    - almost achieved completely
  - Correct known anomalies of the existing SMCS ASICs
  - Goal: Backward compatibility concerning software
  - 3 Volt support

SMCS116/332SpW - New Functions

- Time code (Act as master & Send Time Code)
- Enhanced 32-bit processor support (SMCS116SpW)
  - the protocol engine is modified that it tolerates and executes commands of any length
- FIFO, ADC and UART I/F improved (SMCS116SpW)
- Supports Serial Transfer Universal Protocol (STUP) / PID0xEF
  - SMCS332SpW directs all received data directly to the SW for protocol handling (fully compliant to STUP/RMAP protocol)
  - SMCS116SpW handles optionally all data transfers compliant to the new SpaceWire STUP protocol in hardware
- New header field control bit (SMCS332SpW)
  - Arbitrary packet length, i.e. more flexibility for packet generation

DICOS (Digital Correlator System)

- Used in the MIRAS instrument
- DICOS correlator ASIC has
  27 I-Inputs and 27 Q-Inputs



- Two modes: I with Q and I with I correlation
- The ASIC incorporates 729 correlator cells
- Correlation working with 56MHz, up to 100ms integration

PSIE (Parallel Serial Interface Engine)

- Scalable and flexible high performance Serial Communication Controller for embedded systems
- Packet oriented: Autonomous command execution and protocol generation
- Comprising following (OBC typical) interface functions:
  - 1 SpaceWire link full duplex, up to 200 Mbit/s (in each direction)
  - Service Interface (Debug & Monitor)
  - On-Board Time Function
  - OBC Reconfiguration Logic
  - Similar functionality as SMCS116SpW:
    - RAM-I/F
    - FIFO-I/F
    - etc.
  - Preprocessing of GPS signals
  - Full/Halfduplex HDLC Interfaces

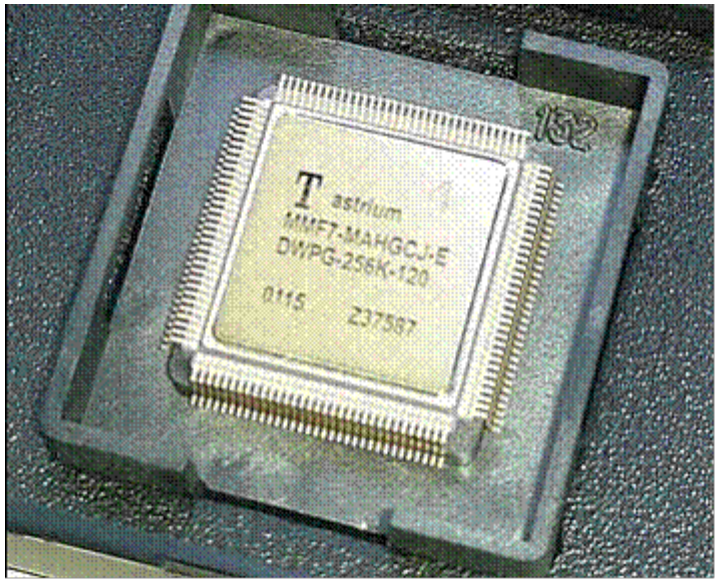
PSIE (Parallel Serial Interface Engine)

- Configurable to work in 5 different operation modes

1. Master Mode: placed on a Processor Module
2. Reconfiguration Mode: placed on an OBC Reconfiguration Module
3. SpW-Remote Mode: placed on remote interface modules (provides similar functionality as SMCS116SpW but with several interfaces in parallel, RAM-I/F, FIFO-I/F, etc.)
4. GPS Mode: placed on Mosaic GNSS receiver
5. HDLC-Remote Mode: placed on a Remote Terminal Module

Wideband Digital Waveform Generator

- Waveform memory segmented into 8 banks 2kx16
- Configurable MUX to resample memory bank buses at 100MHz
- Pulse Switching on a pulse to pulse basis between up to eight pulses.
- Data & Control I/F: Standard µP compatible



TERESA (Telecommand, Telemetry, Re-configuration, Safeguard memory)

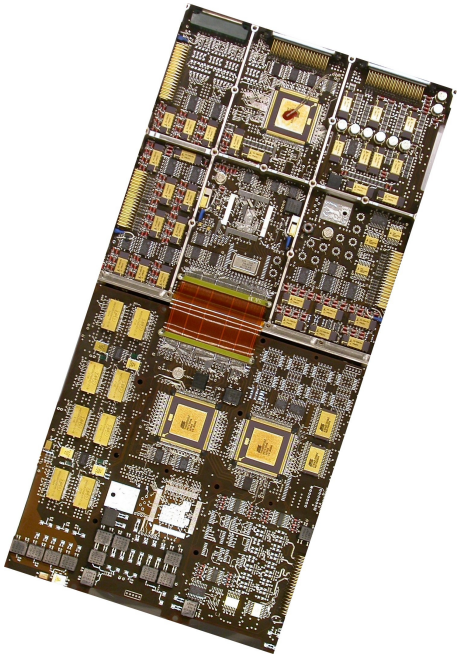
Configurable in 3 different operation modes

- **Communication over Space Wire (including 3 SpW routing function)**

- **1 - Telecommand Mode**
  - Telecommand reception (5 x up to 1MBit/s)
  - Optional decryption
  - PROM configuration
  - Command distribution (CPDU)
  - Surveillance (alarm I/Fs) & Reconfiguration

- **2 - Housekeeping-Memory Mode**
  - SDRAM Housekeeping-Memory up to 32 GBit
  - EDAC SCDD

- **3 - Telemetry Mode**
  - Telemetry transmission (8 channels, up to 20MBit/s)
  - Optional encryption
  - Direct telemetry from internal and external sources
  - Safe Guard & EEPROM Memory I/F (4MByte)
  - External User-interfaces (SpW) for TM downlink
  - Spacecraft elapsed timer (SCET)



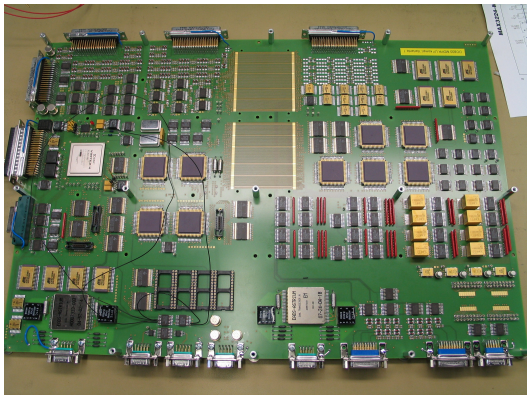
AGGA-3 (Advanced GPS/Galileo ASIC)

- Features On-Chip Processor Part
  - LEON2-FT processor and IEEE-754 compliant FPU (GRFPU)
  - Interrupt controller, processor watchdog, timer
  - DMA controller (dump data between GNSS signal processing core and LEON memory)
  - Debug support
  - SpaceWire links, UARTs
- Features GNSS Part (front-end and beam forming module)
  - GNSS signal processing of up to 36 channels
  - FFT processing module for fast GNSS signal acquisition
  - Support of different input formats (4 baseband inputs)
  - Digital down-conversion on-chip, 8-bit or 3-bit pre-correlation
  - Enhanced power level measurement on all inputs
  - Flexible switching of inputs to all channels
  - Digital beam-forming to form 7 fixed beams

MDPA (Multi-DSP/micro-Processor Architecture)

- LEON2-FT based system-on-chip and including a highly integrated DVB-S modem module

- MDPA includes the following main function and interfaces
  - LEON2-FT and a floating point unit
  - 8 SpaceWire interfaces with routing capability, connected via AMBA and with DMA
  - 2 MilBus (1553) interfaces, connected via AMBA and with DMA
  - 1 CANBus interface, via AMBA
  - 2 Service & Debug I/Fs for Software
  - Embedded Test module
  - Digital modem based on DVB-S codec: data processing for TC & TM control channels of telecommunication payloads



CONCLUSION

- EADS Astrium has significant heritage in the DDV of complex ASICs and FPGAs
  - Presented ASICs are important building blocks in Astriums electronics
- Design of ASICs for a wider community (ASSPs) is essential
- Major concern is, that
  - Safeguarding of current technologies and components receives less weighting than the investment in e.g. latest available technologies.
  - This might lead to a number of components not fully qualified/available (e.g. ASIC technology, VHDL IP cores, devices, …)
- →A clear road map with the international and national agencies is necessary for broad acceptance of the new devices and maturity of new technologies.

→The effort shown by the agencies in this field is highly appreciated!